## REMARKS

Claims 25-30 remain pending. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claim 25 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Ilderem (U.S. Patent No. 5,675,166). Claims 25-26 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Jang (U.S. Patent No. 6,245,620). Claims 26-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ilderem in view of Bai (U.S. Patent No. 5,861,340). These rejections are respectfully traversed.

The present invention is directed at a semiconductor device. Referring to Figs. 4-9 the semiconductor device of the present invention includes an electrode stack 10 disposed upon a dielectric film 16 located over a portion of a wafer, such as substrate 17. The electrode stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls (i.e., the lateral surface of layers 11-15 which comprise the electrode stack 10) 18 of the electrode stack are continuously vertical. A nitride spacer 22 extends along and is in contact with the continuously vertical sidewalls 18, except for the bottom portion, which may be enclosed by an oxide layer 20.

Ilderem is directed to a low voltage field effect transistor (FET). As illustrated in Fig. 10, the FET 20 comprises a gate layer 26 (column 6, line 13) disposed on the surface 22 (column 6, line 2) of a substrate 21 (column 4, line 19). Stacked upon the gate layer

26 is a silicide layer 44 (column 6, line 15). Stacked upon the silicide layer 44 is a gate electrode stack 49 (column 6, line 24). Fig. 10 show that the FET 20 has a different structure than the claimed invention. For example, the claimed invention requires the nitride spacer to be "in contact with" (claim 25) the vertical sidewall of a multi-layer electrode stack. However, the nitride spacers 46 of Ilderem is in contact with an insulating layer, as can be seen by the layer between surfaces 37/38 and the nitride spacer 46. Additionally, the claimed invention further requires the nitride spacer to be "extending along the ... sidewall of the gate electrode stack other than along lowermost portions" (claim 25), while Fig. 10 of Ilderem illustrates the nitride spaces 46 extending along the silicide layer 44 but not along electrode 49.

Jang is directed to a MOS transistor. Fig. 8 illustrates the MOS transistor as comprising a gate pattern 30 disposed over a gate dielectric film 23 located over a substrate 21. The transistor further includes a first dielectric film 31a and a second dielectric film 33a, to form a bi-layer spacer S. Fig. 8 shows the transistor as having a different structure than the claimed invention. In particular, the claimed invention requires a nitride spacer "extending along the ... sidewall of the gate electrode stack other than along lowermost portions," while Fig. 8 illustrates the bi-layer spacer S extending along the entire sidewall of the stack 30.

Bia discloses a semiconductor structure, as illustrated in Bia Fig. 2C. More specifically, the structure includes a gate electrode 222 (column 6, line 18) disposed over a gate dielectric layer 202 (column 3, line 44) located on a substrate 200 (column 3, line

36). The gate electrode 222 includes a top silicide layer 220 (column 6, line 18), a barrier layer 206 (column 3, line 64), and a silicon layer 204 (column 3, line 46). Nearly the entire gate electrode (i.e., all but the very top portion of silicide layer 220) is surrounded by spacer 212. Thus, Bia fails to teach or suggest a structure where a nitride spacer is "extending along the ... sidewall of the gate electrode stack other than along lowermost portions."

As noted, claim 25 recites, "a nitride spacer in contact with and extending along the continuously vertical sidewall of the gate electrode stack other than along lowermost portions of the sidewall." Ilderem, Jang, and Bai are devoid of any teachings or suggestions of a nitride spacer having the recited arrangement. Claim 25 is therefore believed to be allowable over the prior art of record. Claims 26-30 depend from claim 25 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: December 13, 2001

Respectfully submitted,

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**Version With Markings to Show Changes Made**

25. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric film disposed on a surface of the substrate;

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers, each of said plurality of layers including a lateral surface to form a [forming] continuously vertical sidewall[s]; and

a nitride spacer[s] in contact with and extending along the continuously vertical sidewall[s] of the gate electrode stack other than along lowermost portions of the [continuously vertical] sidewall[s].